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(71) Applicant: **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi Kanagawa-ken Tokyo(JP)

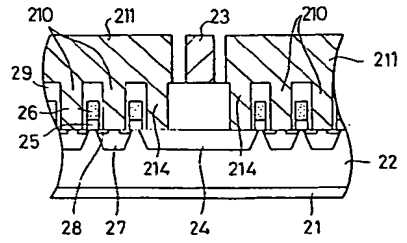
(72) Inventor: **Yoneda, Tatsuo**
D-612, Toshiba-cho 2-1
Futyu-shi, Tokyo(JP)
Inventor: **Suzuki, Kazuaki**
303, Nakasaiwai-cho 4-8,
Saiwai-ku
Kawasaki-shi, Kanagawa-ken(JP)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner,
Patentanwälte,
Arabellastrasse 4
D-81925 München (DE)

(54) Gate wiring of DMOSFET.

(57) A semiconductor device has a first conducting type semiconductor substrate (21 and 22), a plurality of second conducting type first semiconductor regions (27) formed on one part of the surface of the first conducting type semiconductor substrate, a first conducting type high density diffused second semiconductor region (28) formed on one part of the surface within the second conducting type first semiconductor region (27), a gate electrode material (26) extending across one part of the surface of the first conducting type semiconductor substrate (21 and 22), where one part of the surface of the first conducting type high density diffused second semiconductor region, and the second conducting type first semiconductor region (27) are not formed, an insulating film which covers the gate electrode material, a metal source wiring connected to the first conducting type high density diffused second semiconductor region (28), and the second conducting type first semiconductor region (27), a metal gate wiring (23) connected to one part of the surface of the gate electrode material (26) through an open section provided in the insulating film, and a second conducting type third semiconductor regions (24) formed as a plurality of partitions on the surface of the first conducting type semiconductor substrate (21 and 22) on the lower part of the metal gate wiring. In the semiconductor device, the second conducting type third semiconductor region (24) is positioned to approach the limit reached by a depletion layer extending from the second conducting type third semiconductor region (24) to the first conducting type semiconductor substrate (21 and 22).

FIG. 2C



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TECHNICAL FIELD

The present invention relates to a semiconductor device such as a MOS-type transistor or the like used mainly for electrical power, and, in particular, to a semiconductor device, provided with more stable insulation voltage resistance (or an nsulating breakdown voltage) and more stable breakdown voltage (or a drain-source breakdown voltage), which only requires a small amount of fabricating step in the manufacture.

BACKGROUND ART

FIGs.1A to 1D are configuration diagrams of a conventional semiconductor device in the form of a normal power MOSFET.

FIG.1A is a plan view of the periphery of a section of aluminum gate wiring.

FIG.1B is a sectional view (including a source region) when viewed along a section A-A'.

FIG.1C is a sectional view (including a gate region) when viewed along a section B-B'.

FIG.1D is a sectional view (including a source region and no P-type region) when viewed along a section A-A'.

Normally, the peripheral section of the aluminum gate wiring arranged on the surface of the semiconductor has a repetitive structure, therefore a typical section is represented here.

On the surface of a MOSFET for which a high density silicon substrate 1 and a low density silicon substrate 2 act as a drain, first, a gate wiring under the P-type region 4 formed under a gate wiring region (hereinafter referred to as a P-type region) positioned directly under a section of aluminum gate wiring 3 is formed by a special process.

The P-type region 4 provided on the upper surface of the silicon substrate 2 directly under the aluminum gate wiring 3 is formed continuously on the surface of the semiconductor, extending over the gate wiring in the wiring direction C (see FIGs.1A and 1B).

Also, the P-type region 4 is connected to a section of aluminum source wiring 11 on the outer periphery (not shown) of the semiconductor device and has the same source potential.

Next, insulating oxidized gate films 5 are formed as insulating oxidized films, after which silicon gates 6 are formed.

After the desired patterning is performed, the silicon gates 6 are perforated by etching in a unit cell portion.

A P-type base region 7 and a source region 8 are then formed by a self-aligning method to mask an open section of the silicon gate 6.

Finally, holes, specifically contact holes 10 and 12, are opened onto an insulating interlayer film 9 and the elements are connected through aluminum wiring.

The contact hole 10 connects the source region 8 and the P-type base region 7 of each unit cell to aluminum source wiring 11, and the contact hole 12 connects the silicon gate 6 to the aluminum gate wiring 3.

With the gate wiring under-structure of this type of conventional semiconductor device, after the insulating oxidized gate film 5 is formed on the surface of the P-type region 4, impurities from the P-type region 4 become incorporated in the insulating oxidized gate film 5 because the device is passed through various heating processes.

This creates a problem inasmuch as the capability of an insulation voltage registance of the insulating oxidized gate film 5 is reduced.

Normally, as shown in Fig.1B, this problem is avoided by forming the insulating oxidized gate film 5 to an ample thickness in comparison with other film thicknesses, and a special process is necessary to selectively increase the film thickness. In Fig.1B, a depletion layer is indicated by the reference number 13.

On the other hand, as shown in Fig.1D, if the P-type region 4 is absent, a sudden change 14 in the curvature of a depletion layer 13 results because the under-section of the P-type region 4 would normally act as a connecting section for the depletion layer 13 which is formed on both sides of the P-type region 4.

Therefore a localized breakdown is induced from electrostatic concentration so that the breakdown voltage (or a drain-source breakdown voltage between the drain section and the source section) is lowered.

As outlined above, with a conventional semiconductor device having the configuration described above, the problem arises that the insulation voltage resistance of the insulating oxidized gate film is reduced.

This problem is avoided by forming the insulating oxidized gate film to a ample thickness in comparison with other film thicknesses, like the P-type region 4 shown in Fig.1C. However, a special process is necessary to selectively increase the film thickness, which is also a problem.

In addition, as shown in Fig.1D, in the case where there is no P-type region directly under the aluminum gate wiring, the sudden change 14 is caused in the curvature of the depletion layer 13 so that the breakdown voltage (or the drain-source breakdown voltage) is lowered.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is, with due consideration to the drawbacks of such

conventional semiconductor devices, to provide a semiconductor device provided with a high quality insulating film and a more stable voltage resistance by forming a P-type region directly under a section of aluminum gate wiring as partitions, and by forming a unit cell section of the P-type region by the same process.

According to one feature of the present invention, a semiconductor device comprises:

a first conducting type semiconductor substrate;

a plurality of second conducting type first semiconductor regions formed on one part of the surface of said first conducting type semiconductor substrate;

a first conducting type high density diffused second semiconductor region formed on one part of the surface within said second conducting type first semiconductor region;

a gate electrode material extending across one part of the surface of said first conducting type semiconductor substrate, where one part of the surface of said first conducting type high density diffused second semiconductor region, and said second conducting type first semiconductor region are not formed;

an insulating film which covers said gate electrode material;

metal source wiring connected to said first conducting type high density diffused second semiconductor region, and said second conducting type first semiconductor region;

metal gate wiring connected to one part of the surface of said gate electrode material through an open section provided in said insulating film; and

second conducting type third semiconductor regions formed as a plurality of partitions on the surface of said first conducting type semiconductor substrate on the lower part of said metal gate wiring,

wherein said second conducting type third semiconductor region is positioned to approach the limit reached by a depletion layer extending from said second conducting type third semiconductor region to said first conducting type semiconductor substrate.

In the semiconductor device described above, said metal gate wiring connected to the gate electrode material is connected to said open section provided in the insulating film in a part inserted into said second conducting type third semiconductor region.

In addition, in the semiconductor device described above, the diffusion depth of said second conducting type third semiconductor region is equivalent to the diffusion depth of said second conducting type first semiconductor region.

According to another aspect of the present invention, a semiconductor device described above, wherein the spacing between said second conducting type third semiconductor region and said second conducting type first semiconductor region which is adjacent to said second conducting type third semiconductor region is the same as the spacing between said other second conducting type first semiconductor regions.

According to another aspect of the invention, in the semiconductor device, said second conducting type third semiconductor region is connected to the metal source wiring.

According to another aspect of the present invention, in the semiconductor device described above, said second conducting type third semiconductor region and said second conducting type first semiconductor region are formed by the same process.

Moreover, according to another aspect of the invention, in the semiconductor device described above, wherein the distance between adjacent said open sections provided in said insulating film is Ls + Lg, and the distance between adjacent open section which are provided in said insulating film and closed to the second conducting type third semiconductor region is an integer multiple of the length (Ls + Lg) + Ls, where Ls is a width of the open section, and Lg is the width of the gate electrode material.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention will become more apparent from the following description of the preferred embodiments taken in conjunction with the accompanying drawings, in which:

FIG.1A a plan view of the periphery of aluminum gate wiring for a conventional semiconductor device.

FIG.1B is a sectional view (including a source region) when viewed along a section A-A'.

FIG.1C is a sectional view (including a gate region) when viewed along a section B-B'.

FIG.1D is a sectional view (including a source region and no P-type region) when viewed along a section A-A' .

FIG.2A is a plan view of a semiconductor device of the present invention.

FIG.2B and FIG.2C are sectional views (on a source region) when viewed along a section D-D'.

FIG.2B is diagram for explaining a process for forming a P-type base region.

FIG.2C is diagram for explaining a process for forming aluminum wiring.

FIG.3A is a plan view of a semiconductor device of the present invention.

FIG.3B and FIG.3C are sectional views (on a gate contact hole) when viewed along a section E-E'.

FIG.3B is diagram for explaining a process for forming a P-type base region.

FIG.3C is diagram for explaining a process for forming aluminum wiring.

FIG.4A is a diagram for explaining the effect of a gate wiring under-section structure on the gate voltage resistance distribution for a conventional semiconductor device.

FIG.4B is a diagram for explaining the effect of a gate wiring under-section structure on the gate voltage resistance distribution for a semiconductor device of the present invention.

FIG.5A is a diagram for explaining the effect of a gate wiring under-section structure on distribution of a drain-source breakdown voltage (100 [V] system) for a conventional semiconductor device.

FIG.5B is a diagram for explaining the effect of a gate wiring under-section structure on distribution of a drain-source breakdown voltage (100 [V] system) for a semiconductor device of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Other features of this invention will become apparent in the course of the following description of exemplary embodiments which are given for illustration of the invention and are not intended to be limiting thereof.

Embodiments of the present invention will now be explained with reference to the drawings.

Before an explanation of the preferred embodiments of a semiconductor device of the present invention, features of the present invention will be described.

A first feature of an embodiment of the semiconductor device of the present invention, as shown in FIGs.2A to 2C, is that a plurality of second conducting type third semiconductor regions 24 is formed as partitions on the surface of a pair of first conducting type semiconductor substrates 21 and 22 on the under-portion of a section of metal gate wiring 23.

Furthermore, the second conducting type third semiconductor region 24 is positioned to approach the limit reached by a depletion layer 13 extending from the second conducting type third semiconductor region 24 to the first conducting type semiconductor substrates 21, 22.

Specifically, during the formation of the second conducting type third semiconductor region 24 on the under-portion of the metal gate wiring 23, the second conducting type third semiconductor region 24 is formed from a diffusion window opened in a lattice shape in a gate electrode material 26 formed on an insulating film 25.

The quality of the insulating film 25 can be improved, and an insulation voltage resistance(or an insulation breakdown voltage) can be improved.

In addition, the change in curvature of the depletion layer 213 on the lower section of the second conducting type third semiconductor region 24 can be reduced so that more stable breakdown voltage (or a drain-source breakdown voltage) characteristics can be provided.

A second feature of the embodiment of the semiconductor device of the present invention is that the metal gate wiring 23 connected to the gate electrode material 26 is connected at an open section 212 of an insulating film 29 provided on a part inserted into the second conducting type third semiconductor region 24.

For example, as shown in FIG.2A if, when the width of the opening in a silicon gate in a unit cell section is Ls, and the width of the silicon gate between the unit cells is Lg, the spacing of the opening section 212 is centered to equal Ls + Lg, then it is possible to configure the device uniformly.

The fabricating process then becomes simple, and more stable breakdown voltage (or a drain-source breakdown voltage) characteristics can be provided.

A third feature of the embodiment of the semiconductor device of the present invention is that the diffusion depth of the second conducting type third semiconductor region 24 is formed to be equivalent to the diffusion depth of a second conducting type first semiconductor region 27.

As a result, the change in curvature of the depletion layer 213 on the lower section of the second conducting type third semiconductor region 24 can be reduced so that more stable breakdown voltage (or a drain-source breakdown voltage) characteristics can be provided.

A fourth feature of the embodiment of the semiconductor device of the present invention is that the spacing between the second conducting type third semiconductor region 24 and the second conducting type first semiconductor region 27 which is adjacent to the second conducting type third semiconductor region 24 is the same as the spacing between the other second conducting type first semiconductor regions 27.

As a result, it is possible to configure the device uniformly. The manufacturing process then becomes simple, and more stable breakdown voltage (or a drain-source breakdown voltage) characteristics can be provided.

A fifth feature of the embodiment of the semiconductor device of the present invention is that the second conducting type third semiconductor region 24 is connected to a section of aluminum source wiring 211.

As a result, the second conducting type third semiconductor region 24, on which a channel region is not formed, acts as a source electrical potential and can be positively used as a junction diode formed between drain sources.

For example, it is possible to obtain a favorable structure for a destruction mode produced during recovery operation.

Finally, a sixth feature of the embodiment of the semiconductor device of the present invention is that the second conducting type third semiconductor region 24 and the second conducting type first semiconductor region 27 are formed by the same process.

For example, using the same diffusion process, the same diffusion depth is created for the region 24 and the region 27, and by using a shorter process, a semiconductor device with more stable breakdown voltage (or a drain-source breakdown voltage) characteristics can be provided.

FIGs.2A to 2C and FIGs.3A to 3C are configuration diagrams of one embodiment of the semiconductor device of the present invention.

FIG.2A is a plan view of a semiconductor device of the present invention.

FIG.2B and FIG.2C are sectional views (on a source region) when viewed along a section D-D'.

FIG.2B is diagram for explaining a process for forming a P-type base region.

FIG.2C is diagram for explaining a process for forming aluminum wiring.

FIG.3A is a plan view of a semiconductor device of the present invention.

FIG.3B and FIG.3C are sectional views (on a gate contact hole) when viewed along a section E-E'.

FIG.3B is diagram for explaining a process for forming a P-type base region.

FIG.3C is diagram for explaining a process for forming aluminum wiring.

The explanation of this embodiment will be given in relation to an N-channel MOSFET, for convenience.

Also, silicon gates 26 are used in this embodiment because a normal polysilicon is utilized.

A high density silicon substrate 21 and a low density silicon substrate 22 are used as the drain of the MOSFET.

On the surface of the MOSFET, first, an insulated oxidized gate film 25 and the polysilicon gates 26 are formed. Then, diffusion windows 210 and 214 for forming a P-type region 24 are provided by polysilicon etching. At this time, the wiring under-section P-type region diffusion window 214, which is not continuous in the wiring direction, is formed in a plurality of locations on a ladder (see FIG.2A). This is one of the features of the present invention.

In addition, when the silicon gate opening width in the unit cell section is Ls and the silicon gate width between the unit cells is Lg, a diffusion window with a width Ls, an integer multiple of the length (Ls + Lg) + Ls, is arranged at a spacing Ls + Lg, positioned in the shape desired for the wiring under-section P-type region diffusion window 214.

As a result, a maximum effect is obtained because the arrangement of the other FET parts is not disturbed.

Next, P-type regions 24 and 27 are formed by a self-aligning method to mask the polysilicon gates 6 as shown in FIG.2B.

Specifically, The P-type region 24 and the P-type region 27 are formed by the same diffusion process to the same diffusion depth. This is another feature of the present invention.

A source region 28 is formed by conventional technology such as a ion implantation method in each of the unit cells, with the exception of the P-type region 24. No channel region is formed in the P-type region 24.

Finally, an insulating interlayer film 29 is formed on the polysilicon gate 26, a contact hole is opened for connecting the aluminum wiring, and the wiring is installed.

Specifically, the two terminals of the P-type region 24 are connected to aluminum source wiring 211 and connected to a source electrode (see FIG.2C). Also, aluminum gate wiring 23 is connected to the polysilicon gate 26 in a contact hole 212 on the cross-section B-B', inserted into the wiring under-section P-type region diffusion window 14 (see FIG.3C).

Here it is preferable that the gate contact holes 212 be positioned between the wiring under-section P-type region diffusion windows 214 at a spacing of Ls + Lg.

The excellent voltage resistance characteristics of this embodiment of the semiconductor of the present invention will now be explained with reference to FIGs.4A and 4B and FIGs.5A and 5B.

FIGs.4A and 4B are diagrams for explaining the effect of a gate wiring under-section structure on the gate voltage resistance distribution when the thickness of the insulating gate film is 1200 Angstrom.

The distribution is for a number of insulating gate film breakdown voltages [V] when the gate sources or the drain sources are shorted, when applying a voltage across the gate sources.

FIGs.5A and 5B are diagrams for explaining the effect of a gate wiring under-section structure on the drain-source breakdown voltage distribution (100 [V] system).

The distribution is for a number of breakdown voltages [V] when a voltage is applied across the drain sources.

In each case, (1) represents a conventional device; (2) represents a device of the present embodiment.

As shown in FIGs.4A and 4B and FIGs.5A and 5B, as compared to the conventional example, this embodiment shows an improvement in both the insulating gate film breakdown voltage and the breakdown voltage.

In addition, more stable voltage resistant characteristics are obtained.

The above-mentioned embodiment was explained for an N-channel MOSFET, but obviously the present invention can also be applied to all other MOS-type transistors such as a P-channel MOSFET, or an IGBT (Insulated Gate Bipolar Transistor).

Also, polysilicon was used in the above explanation as a structural member for purposes of convenience only and is not limitative of the present invention which can be applied to all silicon gates.

By means of the present invention as outlined above, the second conducting type third semiconductor region of the metal gate wiring under-section is formed from the diffusion window opened in a lattice shape in the gate electrode material formed on the insulating film, therefore the quality of the insulating film can be improved and the insulation voltage resistance (or the drain-source breakdown voltage) can be improved.

In addition, the change in curvature of the depletion layer on the lower section of the second conducting type third semiconductor region can be reduced so that a semiconductor device with more stable breakdown voltage (or the drain-source breakdown voltage) characteristics can be provided.

Also, by means of the present invention, the metal gate wiring connected to the gate electrode material is connected at the open section of the insulating film provided on a part inserted into the second conducting type third semiconductor region, and the open section is positioned so as to be evenly space around the center, so that the device is evenly spaced.

The manufacturing process then becomes simple, and a semiconductor device with more stable breakdown voltage (or the drain-source breakdown voltage) characteristics can be provided.

Also, by means of the present invention, the diffusion depth of the second conducting type third semiconductor region is formed to be equivalent to the diffusion depth of the second conducting type first semiconductor region. Therefore, the change in curvature of the depletion layer on the lower section of the second conducting type third semiconductor region can be reduced so that a semiconductor device with more stable breakdown voltage (or the drain-source breakdown voltage) characteristics can be provided.

By means of the present invention, the spacing between the second conducting type third semiconductor region and the adjacent second conducting type first semiconductor region is the same as the spacing between the other second conducting type first semiconductor regions. As a result, it is possible to configure the device uniformly.

The manufacturing process then becomes simple, and a semiconductor device with more stable breakdown voltage (or the drain-source breakdown voltage) characteristics can be provided.

Also, by means of the present invention, the second conducting type third semiconductor region is connected to the aluminum source wiring, and, the second conducting type third semiconductor region, on which a channel region is not formed, acts as a source potential so that it can be positively used as a junction diode formed between drain sources.

For example, it is possible to provide a semiconductor device with a favorable structure for a destruction mode produced during recovery.

In addition, by means of the present invention, the second conducting type third semiconductor region and the second conducting type first semiconductor region are formed by the same process. For example, with the same diffusion process, the same diffusion depth is created for the regions, and a semiconductor device with more stable breakdown voltage (or the drain-source breakdown voltage) characteristics can be provided by the use of a shorter process.

Claims

1. A semiconductor device comprising:

a first conducting type semiconductor substrate (21 and 22);

a plurality of second conducting type first semiconductor regions (27) formed on one part of the surface of said first conducting type semiconductor substrate (21 and 22);

a first conducting type high density diffused second semiconductor region (28) formed on one part of the surface within said second conducting type first semiconductor region (27);

a gate electrode material (26) extending across one part of the surface of said first

conducting type semiconductor substrate (21 and 22), where one part of the surface of said first conducting type high density diffused second semiconductor region (28), and said second conducting type first semiconductor region (27) are not formed;

an insulating film (29) which covers said gate electrode material (26);

metal source wiring (211) connected to said first conducting type high density diffused second semiconductor region (28), and said second conducting type first semiconductor region (27);

metal gate wiring (23) connected to an open section provided in said insulating film (25 and 29) on one part of the surface of said gate electrode material (26); and

second conducting type third semiconductor regions (24) formed as a plurality of partitions on the surface of said first conducting type semiconductor substrate (21 and 22) on the lower part of said metal gate wiring (23),

wherein said second conducting type third semiconductor region (24) is positioned to approach the limit reached by a depletion layer (213) extending from said second conducting type third semiconductor region (24) to said first conducting type semiconductor substrate (21 and 22).

2. A semiconductor device as claimed in claim 1,

wherein said metal gate wiring connected to the gate electrode material is connected to said open section provided in the insulating film in a part inserted into said second conducting type third semiconductor region.

3. A semiconductor device as claimed in claim 1 or 2,

wherein the diffusion depth of said second conducting type third semiconductor region is equivalent to the diffusion depth of said second conducting type first semiconductor region.

4. A semiconductor device as claimed in any one of claims 1 to 3,

wherein the spacing between said second conducting type third semiconductor region and said second conducting type first semiconductor region which is adjacent to said second conducting type third semiconductor region is the same as the spacing between said other second conducting type first semiconductor regions.

5. A semiconductor device as claimed in any one of claims 1 to 4,

wherein said second conducting type third semiconductor region is connected to the metal source wiring.

6. A semiconductor device as claimed in any one of claims 1 to 5,

wherein said second conducting type third semiconductor region and said second conducting type first semiconductor region are formed by the same process.

7. A semiconductor device as claimed in claim 1,

wherein the distance between adjacent said open sections provided in said insulating film is Ls + Lg, and the distance between adjacent open section which are provided in said insulating film and closed to the second conducting type third semiconductor region is an integer multiple of the length (Ls + Lg) + Ls, where Ls is a width of the open section, and Lg is the width of the gate electrode material.

FIG. 1A

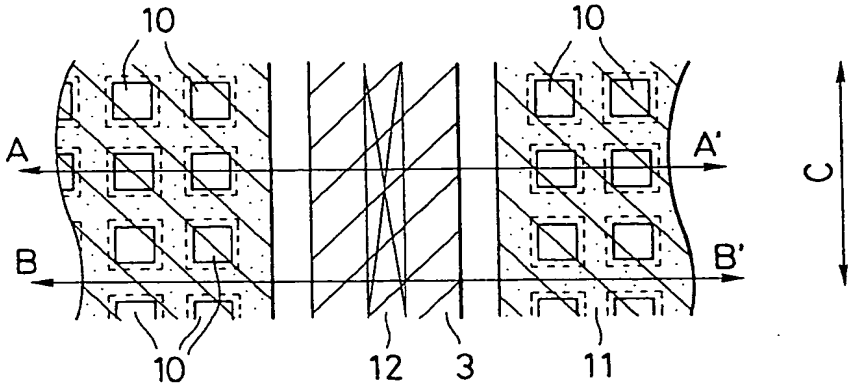


FIG. 1B

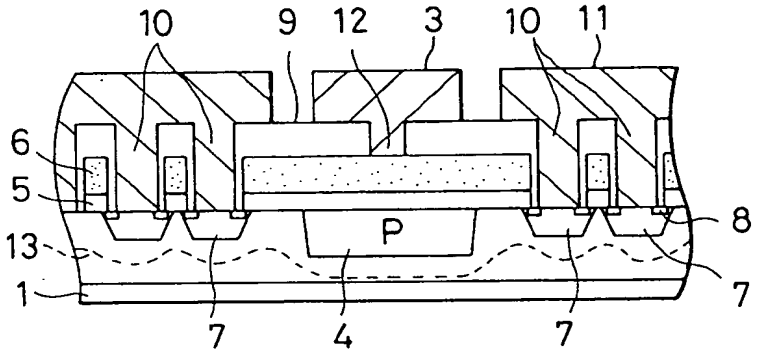


FIG. 1C

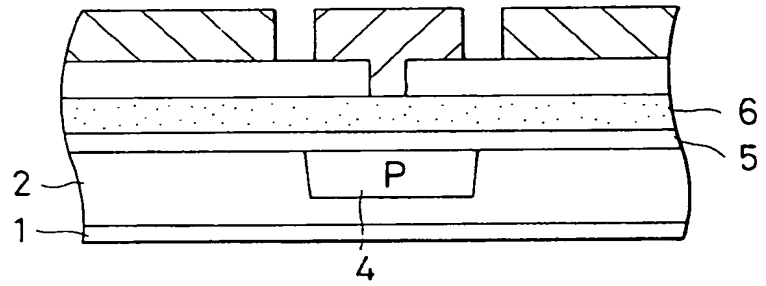


FIG. 1D

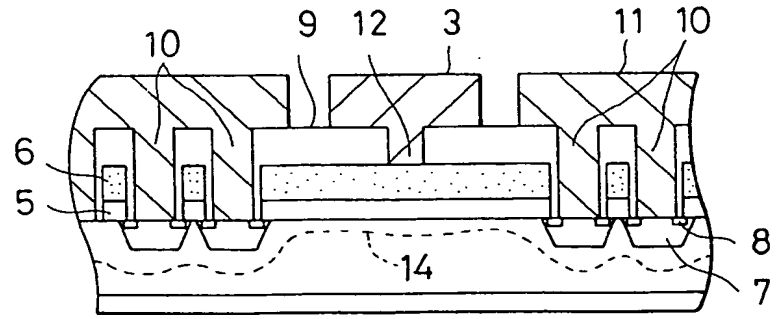


FIG. 2A

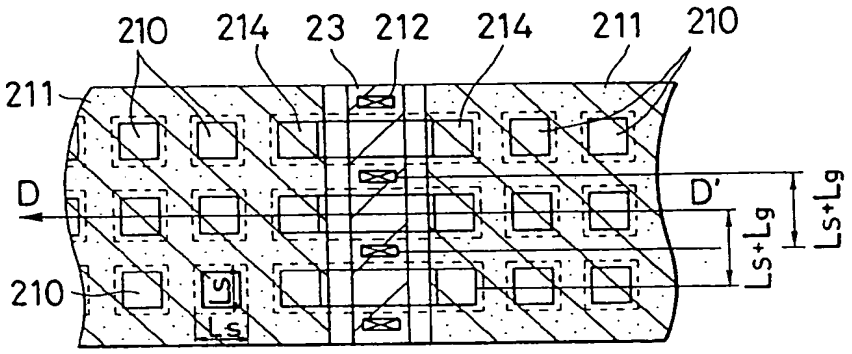


FIG. 2B

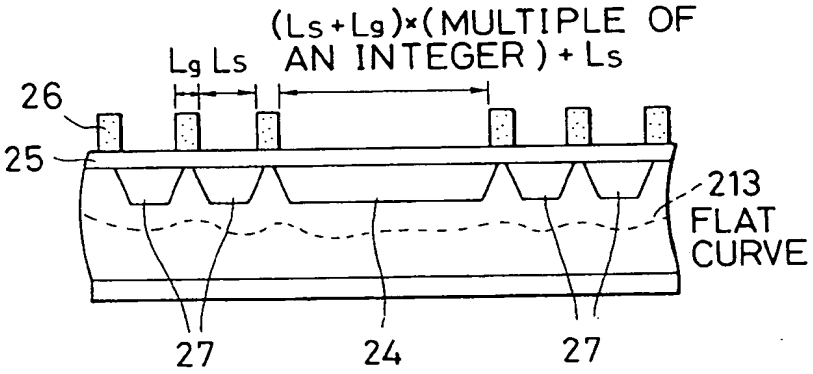


FIG. 2C

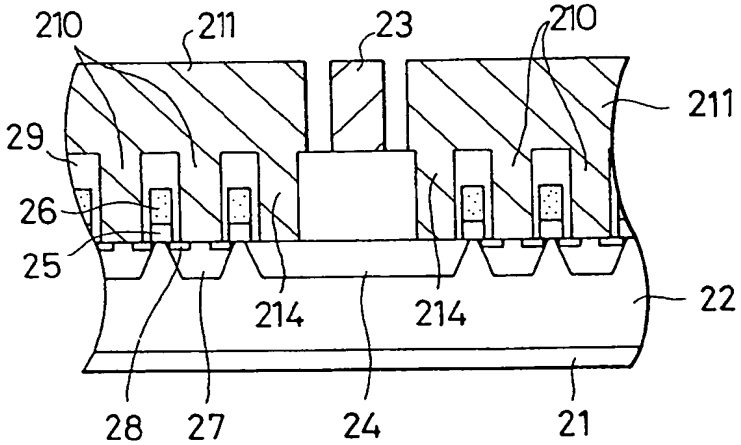


FIG. 3A

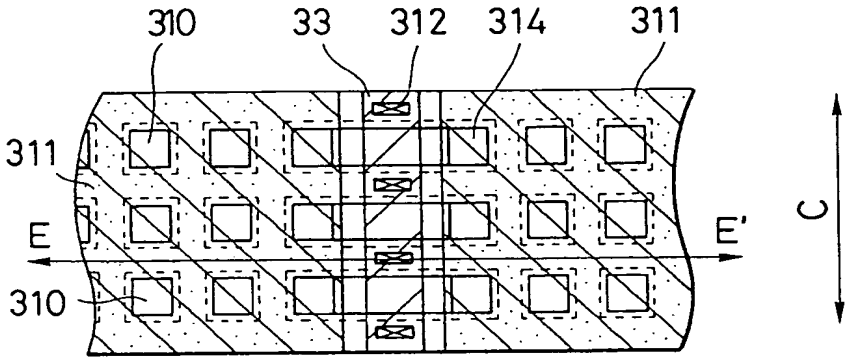


FIG. 3B

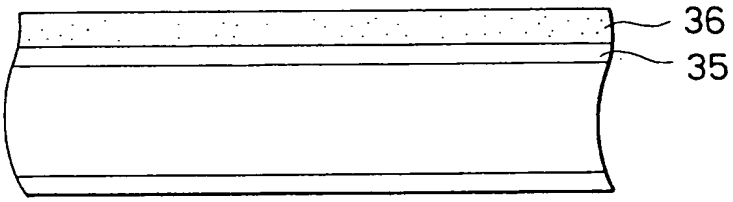


FIG. 3C

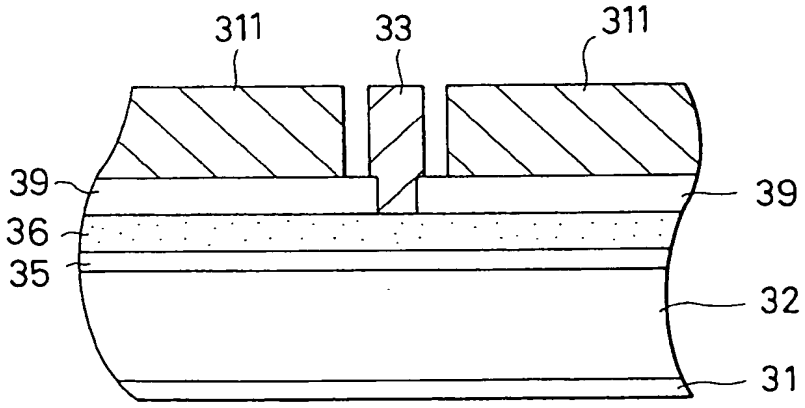


FIG. 4A FIG. 4B

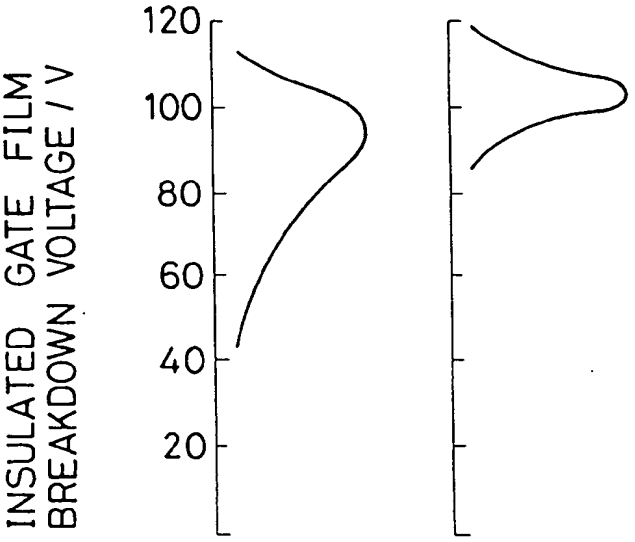
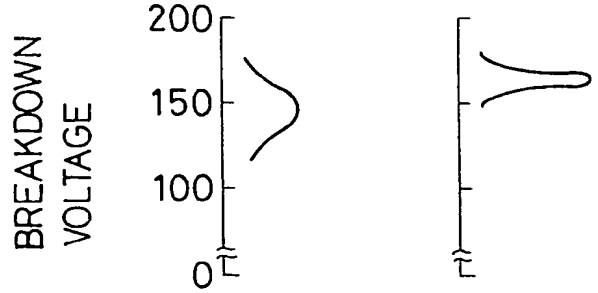


FIG. 5A FIG. 5B



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(71) Applicant: KABUSHIKI KAISHA TOSHIBA
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi Kanagawa-ken Tokyo(JP)

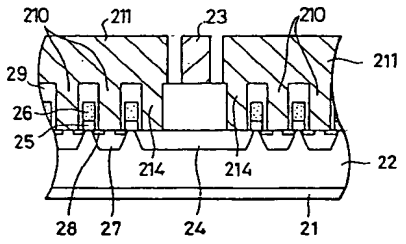
(72) Inventor: Yoneda, Tatsuo
D-612, Toshiba-cho 2-1
Futyu-shi, Tokyo(JP)
Inventor: Suzuki, Kazuaki
303, Nakasaiwai-cho 4-8,
Saiwai-ku
Kawasaki-shi, Kanagawa-ken(JP)

(74) Representative: Lehn, Werner, Dipl.-Ing. et al
Hoffmann, Eitle & Partner,
Patentanwälte,
Arabellastrasse 4
D-81925 München (DE)

(54) Gate wiring of DMOSFET.

(57) A semiconductor device has a first conducting type semiconductor substrate (21 and 22), a plurality of second conducting type first semiconductor regions (27) formed on one part of the surface of the first conducting type semiconductor substrate, a first conducting type high density diffused second semiconductor region (28) formed on one part of the surface within the second conducting type first semiconductor region (27), a gate electrode material (26) extending across one part of the surface of the first conducting type semiconductor substrate (21 and 22), where one part of the surface of the first conducting type high density diffused second semiconductor region, and the second conducting type first semiconductor region (27) are not formed, an insulating film which covers the gate electrode material, a metal source wiring connected to the first conducting type high density diffused second semiconductor region (28), and the second conducting type first semiconductor region (27), a metal gate wiring (23) connected to one part of the surface of the gate electrode material (26) through an open section provided in the insulating film, and a second conducting type third semiconductor regions (24) formed as a plurality of partitions on the surface of the first conducting type semiconductor substrate (21 and 22) on the lower part of the metal gate wiring. In the semiconductor device, the second conducting type third semiconductor region (24) is positioned to approach the limit reached by a depletion layer extending from the second conducting type third semiconductor region (24) to the first conducting type semiconductor substrate (21 and 22).

FIG. 2C



EP 0 587 176 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 93 11 4567

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
P,X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 337 (E-1388)25 June 1993 & JP-A-05 041 523 (OKI ELECTRIC IND CO LTD) 18 February 1993 * abstract * ---	1-7	H01L29/784 H01L29/60 H01L29/10
A	PATENT ABSTRACTS OF JAPAN vol. 5, no. 159 (E-77)14 October 1981 & JP-A-56 088 362 (TOKYO SHIBAURA DENKI K.K.) 17 July 1981 * abstract * ---	1-7	
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 187 (E-0917)16 April 1990 & JP-A-02 035 780 (MATSUSHITA ELECTRON CORP) 6 February 1990 * abstract * ---	1-7	
A	PATENT ABSTRACTS OF JAPAN vol. 006, no. 254 (E-148)14 December 1982 & JP-A-57 153 468 (TOKYO SHIBAURA DENKI KK) 22 September 1982 * abstract * ---	1-6	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L
A	EP-A-0 279 403 (NEC CORPORATION) * abstract; figure 1 * -----	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 February 1994	Mimoun, B

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